08/789,421





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Ø8/789,421	01/29/97	HARARI.	E	
		24M1/0908	EXAMINER	
GERALD P PARSONS MAJESTIC PARSONS SIEBERT & HSUE			HUA, L	
FOUR EMBARCA			ART UNIT	PAPER NUMBER
SUITE 1100 SAN FRANCISO		•	2413	6
			DATE MAILED:	09/08/97

This is a communication from the examiner in charge of your application. COMMISSIONER OF PATENTS AND TRADEMARKS

1	'his a	application has been examined Responsive to communication filed on January 2, This action is made final.		
A shortened statutory period for response to this action is set to expire month(s), days from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133				
Part	ı	THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:		
1.		Notice of References Cited by Examiner PTC-892		
3.	Щ	Notice of Art Cited by Applicant, PTO-1449.		
5.	Ш	Information on How to Effect Drawing Changes, PTO-1474.		
Part (•	SUMMARY OF ACTION		
1.	3	Claims are pending in the application.		
		Of the above, claims are withdrawn from consideration.		
9	ГZ	Claims have been cancelled.		
_		have been cancelled.		
, 3.		Claims are allowed.		
_	-	51-601		
4.	۳	Claims 56-62 are rejected.		
5.		Claims are objected to.		
6.	Ц	Claims are subject to restriction or election requirement.		
7.				
•••	_	This application has been filed with informal drawings under 37 C.F.R. 1.85 which are acceptable for examination purposes.		
8.		Formal drawings are required in response to this Office action.		
9.	$\overline{}$	••••••••••••••••••••••••••••••••••••••		
v.	ш	The corrected or substitute drawings have been received on Under 37 C.F.R. 1.84 these drawings are acceptable not acceptable (see explanation or Notice re Patent Drawing, PTO-948).		
10.		The proposed additional or substitute sheet(s) of drawings, filed on has (have) been approved by the		
		examiner. disapproved by the examiner (see explanation).		
11.	П	The proposed drawing correction filed as		
•••	_	The proposed drawing correction, filed on, has been _ approved disapproved (see explanation).		
12.		Acknowledgment is made of the claim for priority under U.S.C. 119. The certified copy has been received not been received		
		been filed in parent application, serial no; filed on		
13.		Since this application appears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in		
		accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.		
14.		Other		
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Serial Number: 08/789,421

Art Unit: 2413

- 1. The drawings are objected to under 37 C.F.R. § 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore the following elements must be shown or the feature canceled from the claims:
 - a. the "standard power supply" recited in claim 56,
 - b. the "individually addressable storage cells" recited in claim 56,
 - c. the "spare storage cells" recited in claim 56
 - d. the "means for erasing" recited in claim 56,
 - e. the "means for reading" recited in claim 56,
 - f. the "means for programming" recited in claim 56, and
 - g. the "means for substituting" recited in claim 56;
 - h. the "means for initially programming" recited in claim 57,
 - i. the "means for initially determining" recited in claim 57, and
 - i. the "means for writing" recited in claim 57;
 - k. the "spare sectors" recited in claim 58;
 - 1. the "means for performing error correction" recited in claim 59;
 - m. the "standard magnetic disk drive storage system" recited in claim 60;
 - n. the "means for operating" recited in claim 61, and
 - o. the "standard power supply" recited in claim 61; and
 - p. the "means for generating voltages" recited in claim 62,
 - q. the "means for error correction" recited in claim 62, and
 - r. the "storage system" recited in claim 62.

Serial Number: 08/789,421

Art Unit: 2413

The applicant is requested to be consistent in usage of terminology so that terms used in claims can be readily seen in the drawings. No new matter should be entered.

Page 3

2. Applicant is required to submit a proposed drawing correction in response to this Office action.

3. The disclosure is objected to because of the following informalities: at page 5, lines 11-12, intended correction has not been made clear and not initialized at the margin by the person who made the intended correction. Appropriate correction is required.

4. Claims 56-62 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. As per claim 56;

At line 4, it appears that a noun is missing between the words "following" and "mounted".

b. As per claim 57:

The applicant is requested to delete the word "which" at line 2.

c. As per claim 58:

At line 6, it appears that the word "sector" should be changed to --sectors--.

d. As per claim 59;

Art Unit: 2413

This claim is incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2173.05(l). The Connections for the means for performing error correction have not been recited and thus its cooperation with other elements is considered incomplete.

e. As per claim 60;

- i. It is not clear how the controller and the interface are connected to the system bus. It is not clear whether both the controller and the interface are directly connected to the system bus, the controller connected to the interface then the interface is connected to the system bus or the interface is connected to the controller then the controller is connected to the system bus.
- ii. At line 6, "said disk drive system" lacks proper antecedent basis.

f. As per claim 62:

- i. At lines 3 and 5, the phrase "the operation" lacks antecedent basis because the EEprom chips might have various operations and it is not clear which one of the various operations is referred to by the phrase.
- ii. At lines 7, the phrase "the operation" lacks antecedent basis because the storage system might have various operations and it is not clear which one of the various operations is referred to by the phrase.

Art Unit: 2413

5. Claim 62 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. The previous claim 56 claims a memory card; but claim 62 claims a storage system. Since claim 62 claims a different invention, claim 62 does not further limit the subject matter of the previous claim.

6. The following is a quotation of 35 U.S.C. § 103 which forms the basis for all obviousness rejections set forth in this Office action:

A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. § 103, the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 C.F.R. § 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of potential 35 U.S.C. § 102(f) or (g) prior art under 35 U.S.C. § 103.

Art Unit: 2413

8. Claims 56 and 58 are rejected under 35 U.S.C. § 103 as being unpatentable over Fukushi et al. (4,757,474, hereafter referred to as Fukushi) in view of Rao (4,949,309) and common practices in the art.

a. As per claims 56 and 58:

 Fukushi discloses the memory device substantially as claimed including means for substituting spare storage cells for storage cells that cannot be addressed.

The Fukushi's storage cells are organized into a plurality of groups (or sectors) each of which contains a plurality of storage cells.

It is inherent that the disclosure of Fukushi is associated with a computer system which is connected to an address bus lines which are connected to the memory device.

ii. However, Fukushi's memory device does not show a plurality of chips of EEPROM type. This is because: (a) Fukushi's regular and spare memory cells are of general type and are not limited to EEPROM type and (b) those cells are plentiful enough that a plurality of the combination of Fukushi's elements 1 and 7 and memory expansion are not necessary.

Art Unit: 2413

iii. Rao teaches a plurality of EEPROM memory cells which are partitioned into groups (or sectors) each of which groups comprises a plurality of storage cells that can be individually addressed for individually programming and erasing each of the storage cells without disturbing the other storage cells.

- iv. Official Notice is, hereby, taken that:
 - (1) it is a common practice in the art to provide a memory device (such as an EEprom) with the necessary means such as:
 - (a) means for erasing memory cells,
 - (b) means for programming memory cells, and
 - (c) means for reading the content of memory cells; and
 - (2) it is a common practice in the art to add memory chips to increase memory size.
- v. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to apply both Fukushi's teaching of substituting spare storage cells for regular storage cells and Rao's teaching of using EEPROM cells as a storage cells to design memory device having Rao's EEPROM cells and Fukushi's means for substituting spare storage cells for regular storage cell.

Art Unit: 2413

vi. The person having ordinary skill in the art would have been motivated to combine the teachings of Rao and Fukushi because the person would wish to substitute a spare storage cell for a regular storage cell when the regular storage cell cannot be acted on as taught by Fukushi and because that person would know that EEPROM cells are like any other kind of memory cells are some time cannot be acted on (due to defect).

b. As per claim 61:

- i. Official notice is taken that it is a common practice in the to provide various operating voltages for operating the various operations on an EEPROM and it is also a common practice in the art to provide a necessary voltage regulating means for generating various operating voltages from a power supply to supply the various operating voltages to operate the EEPROM.
- ii. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to provide various EEPROM operating voltages to various operations of an EEPROM because the various operations of the EEPROM do require various operating voltages.

c. As per claim 57:

 Official notice is taken that transferring data to a memory device through a cache is a common practice in the art.

Art Unit: 2413

ii. It would have been obvious to one having ordinary skill in the art at the time the invention was made to write data to a cache prior to write it into a memory device because in this way the memory device might be slow at it writing operation and because the source which sends the data cannot afford to wait.

- The person having ordinary skill in the art would have been motivated to write data to a cache prior to writing it to a memory device because it would enhance processing time efficiency at the source which sends the data.
- 9. Claim 59 is rejected under 35 U.S.C. § 103 as being unpatentable over Fukushi et al. (4,757,474) hereafter referred to as Fukushi), Rao (4,949,309) and common practice in the art as applied to claims 56 and 58 above and further in view of Takemae (4,688,219).

As per claim 59:

- Takemae teaches a means for correcting those error which can be corrected by using error correction codes.
- ii. It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teaching of Takemae with the teachings of Rao and Fukushi to add an error correction means into the obvious memory device which has been addressed above in the rejection of claim 56 and 58.

Art Unit: 2413

iii. formed that comprises a means for correcting error so that data read out from the memory can be corrected.

- iv. One having ordinary skill in the art would have been motivated to add, in addition to the means for substituting spare bits for faulty regular bits, an error correction circuit to a memory card **because** one would consider a situation of soft error as taught by Takemae.
- 10. Claim 60 is rejected under 35 U.S.C. § 103 as being unpatentable over Fukushi et al. (4,757,474) hereafter referred to as Fukushi), Rao (4,949,309) and common practice in the art as applied to claim 56 above and further in view of Tuma et al (5,070,474 hereinafter referred to as Tuma).

As per claim 60:

- i. A controller (i.e., the SMD disk controller, which see a solid state memory as a disk), which is interfaced with a solid state memory, for responding to commands sending to a disk and for controlling the solid state memory (col. 4, lines 9-37).
- ii. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to add Tuma's controller to the modified memory device of Fukushi.
- iii. The artisan would have been motivated to add Tuma's controller to the modified memory device of Fukushi because:

Art Unit: 2413

(1) Fukushi's memory device is of solid state type;

(2) Tuma's memory is of solid state type; and

(3) The addressing of the solid state memory of Fukushi is similar to

the addressing of the solid state memory of Tuma as it is expected

in the art of addressing solid state memories.

11. The prior art made of record and not relied upon is considered pertinent to applicant's

disclosure.

12. Although the references cited in PTO FORM-1449 are available in the prior patent

applicantions that are parents to the present application and have been considered, the copies of

these reference (especially the nonU.S. patent documents) are needed for the present application.

The applicant is requested to furnish those references.

13. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks Washington, D.C. 20231

or faxed to:

(703) 308-9051, (for formal communications intended for entry)

Or:

(703)305-9724 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Art Unit: 2413

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Ly Hua whose telephone number is (703) 305-9684. The examiner can normally be reached on Monday to Friday from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Robert W. Beausoliel, Jr., can be reached on (703) 305-9713. The fax phone number for this Group is (703) 305-9742.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

LY V. HUA
PATENT EXAMINER
ART UNIT 2413

L. Hua August 17, 1997